REMARKS

Claims 1-13 are pending in the application. Claim1 has been amended to more particularly point out and claim the invention. In particular, claim 1 has been amended to incorporate subject matter recited in original claim 10 to clarify that the invention comprises both a via passage, having a first depth, as well as an alignment recess, having a second depth. Support for the amendment of claim 1 is found at least in original claim 10; in the original specification at page 5, lines 3-11; page 6, line 23 through page 7, line 4; and in original Figs. 4a-4d. Claim 10 has been amended to delete subject matter incorporated into claim 1 in the present amendment. Claim 13 has been amended to address an objection of the Examiner and to provide correct claim dependency. No new matter has been added by the foregoing amendments.

Objection to the Claims

The Examiner has objected to claim 13 for certain informalities associated with an antecedent basis issue. Claim 13 has been amended to depend from claim 10 rather than claim 9. Applicant respectfully submits that with this amendment, the antecedent basis issue has been corrected. Applicant respectfully requests that the Examiner's objections to the claims be withdrawn.

Claim Rejections – 35 U.S.C. § 102 – claims 1, 2, and 3

The Examiner has rejected claims 1, 2, and 3 under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,599,809 (Anma *et al.*, hereinafter "Anma"). In view of the amendment of claim 1, Applicants respectfully traverse these rejections of claims 1-3 under 35 U.S.C. § 102(e).

Claim 1 has been amended to incorporate subject matter from claim 10. In particular, claim 1, as amended, is directed to a method for forming an alignment mark structure for a semiconductor device, and recites, *inter alia*:

> ...
> forming a via passage (128) **having a first depth** at a selected level of a substrate of the semiconductor device;

> forming an alignment recess (130) **having a second depth greater than the first depth** at the selected level of the semiconductor device substrate;
>
> forming a first metal layer (140) over said selected substrate level, within said via passage and within said alignment recess (130), wherein said via passage (128) is at least substantially filled with the first metal layer (140), and wherein said alignment recess (130) is only partially filled by said first metal layer (140);
>
> forming a second metal layer (142) over said first metal layer (140) such that said alignment recess (130) is completely filled; .... (Emphasis added.)

Claim 10 was rejected under 35 U.S.C. § 103(a) based upon a combination of Anma and prior art (Fig. 3a) disclosed in the present application. In relying upon a combination Anma and Fig. 3a to reject claim 10, the Examiner admits that Anma alone fails to disclose the feature, now claimed in claim 1, of an alignment recess formed at a greater depth than a depth of a via passage.

Initially, Applicant notes that as Anma alone fails to disclose at least the feature of an alignment recess formed at a greater depth than a depth of a via passage as claimed in claim 1, it is respectfully submitted that a *prima facie* case for anticipation has not been established with respect to claim 1, as amended, or claims 2 and 3 depending from claim 1. Accordingly, it is respectfully requested that the rejection of claims 1-3 under 35 U.S.C. § 102(e) be withdrawn.

Additionally, given that rejection of claim 10 under 35 U.S.C. § 103(a) is now relevant to claim 1, as amended, the rejection of claim 10 will be discussed presently relative to amended claim 1.

In rejection of claim 10, the Examiner has relied upon Fig. 3a of the present application, disclosed to be prior art, to disclose the feature claimed in original claim 10 (as well as amended claim 1) of an alignment recess being formed at a greater depth than a depth of a via. The Examiner asserts that it would have been obvious to one of ordinary skill in the art to make the alignment mark of Anma deeper than the via so that the mark would be visible after the deposition process.

Anma discloses a method of manufacturing a marking recess in a semiconductor device. In particular, with reference to Figs. 22 and 23 as well as the specification at column 1, lines 29-56, Anma discloses as prior art an insulating film 101 having a contact hole 103 and a marking recess 102. Anma further discloses a manufacturing step in which a barrier metal film 104 is deposited to cover sides and a bottom of the contact hole 103 as well as to cover sides and a bottom of marking recess 102. In a subsequent manufacturing step, a tungsten film 105 is deposited over the barrier metal film 104 to fill the contact hole 103. However since "width W2 of marking recess 102 is much greater than width W1 of contact hole 103, marking recess 102 still has an opening reflecting the geometry of marking recess 102 even after tungsten film 105 is provided". Column 1, lines 48-51. Anma thus discloses marking recesses which are much wider than contact holes.

With reference to Figs. 1-21 and the specification at column 7, line 65 to column 14, line 24, Anma further discloses interlayer insulating film 1, contact hole 3, and trench 2. Anma discloses a barrier metal film 4 and a tungsten film 5. These elements 1-5 correspond to the prior art elements 101-105, respectively. In a first embodiment, Anma still further discloses a resist film 6 which is deposited to fill a void left in trench 2 following deposition of tungsten film 5. In a second embodiment, Anma discloses use of a spin-on-glass material 10 to fill the trench 2, rather than the resist film 6. In a third embodiment, Anma discloses use of a silicon oxide film 13 to fill the trench 2, rather than the resist film 6. In a fourth embodiment, an opaque spin-on-glass material 15 is used to fill the trench 2. In a fifth embodiment, trench 2 is replaced by a wider trench 19, and resist film 6 is again used to fill trench 19 subsequent to deposition of tungsten film 5. In a sixth embodiment, a trench 20, again wider than trench 2, is filled using spin-on-glass material 10. In a seventh embodiment, upper surfaces 12 of the barrier metal films 4a and 4b and tungsten films 5a and 5b extend beyond an upper surface 11 of the interlayer insulating film 1. In an eighth embodiment, an overlying interlayer insulating film 18 is provided, having an upper surface which is substantially level with upper surface 12 of the tungsten films 5a and 5b, and barrier metal films 4a and 4b.

Anma thus discloses a high aspect ratio (aspect ratio being the ratio of height to width) contact hole 2 which is substantially more narrow than marking recess 3. See Figs. 1-21. See

also the specification of Anma, for example, at column 5, lines 33-35. In reading the specification, the person of ordinary skill in the art would immediately recognize that Anma specifically contemplates that the marking recess 3 is sufficiently wider than the contact hole 2 such that in the step of depositing the tungsten film 5, the contact hole 2 fills from the sides, while the marking recess is sufficiently wider than the contact hole 2 such that following deposition of the tungsten film, a void remains in the marking recess 3. If the marking recess 3 were substantially the same width (or less) as the contact hole 2, then the marking recess 3 would be filled following deposition of the tungsten film, which would defeat the objective of Anma of ultimately forming a void to mark a location on a semiconductor device.

Fig. 3a of the present application, relied upon by the Examiner, discloses as prior art a semiconductor device having a via opening 128 and an alignment recess 130. The alignment recess 130 is disclosed to be formed deeper than the via 128. Figs. 3a-3d and Figs. 4a-4d disclose the alignment recess 130 having a width which is substantially the same as a width of the via opening 128.

When making a rejection under 35 U.S.C. § 103, the Examiner has the burden of establishing a *prima facie* case of obviousness. The Examiner satisfies this burden only by showing: (1) some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (2) a reasonable expectation of success, and (3) the prior art references much teach or suggest all of the claim limitations (see MPEP 706.02(j)). The teaching or suggestion to make the claim combination and reasonable expectation of success must be found in the prior art and not from the applicant's disclosure (see MPEP 706.02(j)).

Anma and the prior art of Fig. 3a are not properly combinable under 35 U.S.C. § 103(a). The Examiner has asserted that it would have been obvious to one of ordinary skill in the art to make the alignment mark deeper than the via used to contact an underlying metal so that the mark would be visible after the deposition process. Applicant respectfully disagrees. Clearly, the invention of Anam by itself discloses a marking recess which is visible (or, perhaps more accurately, "detectable") after a deposition process. Providing a detectable recess is clearly a

central objective of Anam's invention. Similar to the process of Figs. 3a-3d, the invention of Anam provides a marking or alignment recess that includes a void (that would be detectable on the upper surface of the semiconductor device). Contrary to the Examiner's assertion, the artisan would fail to recognize any motivation to combine the alignment recess of Fig. 3a with the marking recess of Anam for the purpose of providing a visible mark, because the marking recess of Anam is already disclosed to be visible or detectable following the deposition process.

Moreover, the person of ordinary skill in the art would recognize that the prior art illustrated by Fig. 3a is directed to an approach for forming an alignment recess for use in conjunction with relatively low aspect ratio vias, while Anam is directed to an approach for forming a marking recess for use in conjunction with relatively high aspect ratio vias. With respect to Fig. 3a, as via passage 128 and alignment recess 130 are disclosed to be substantially the same width (and thus both the via passage 128 and the alignment recess 130 fill from the bottom, rather than from the sides as the contact hole 2 of Anma), formation of the void in alignment recess 130 following deposition of first metal film 140 **requires** that the alignment recess 130 be deeper than the via passage 128. Stated otherwise, the via passage 128 of the present invention is disclosed to have a relatively low aspect ratio in contrast to the relatively high aspect ratio of the contact hole 2 disclosed by Anam. Accordingly, via passage 128 tends to fill from its bottom when metal film 140 is deposited. In order for there to be a void in alignment recess 130 following deposition of tungsten film 140, it is necessary that alignment recess 130 be deeper than via passage 128.

Both Anma and the process of Figs. 3a-3d culminate in providing an alignment or marking recess. Anma is clearly and specifically directed to a process wherein a marking recess void is formed by providing a marking recess which is wider than a high aspect ratio contact hole. The process of Figs. 3a-3d is equally clearly and specifically directed to a process wherein a void is formed in an alignment recess by providing an alignment recess which is deeper than a relatively low aspect ratio contact hole. The artisan, having both the disclosure of Anma and Fig. 3a before him or her, would fail to recognize any teaching, suggestion, or motivation to combine the deep marking recess of Fig. 3a (suitable for use with a low aspect ratio via) with the wide marking recess of Anma (suitable for use with a high aspect ratio via). Such a combination

would be pointless, as the process of Anma and the process of Fig. 3a are separately suitable for use with one of two different structures. Absent any teaching, suggestion, or motivation to make the proposed combination, the proposed combination of Anma and Fig. 3a is not proper under 35 U.S.C. 103(a).

Neither combination nor modification of Anam and the disclosure of Fig. 3a is taught or suggested by the prior art. It is therefore respectfully submitted that a *prima facie* case for obviousness has not been established with respect to claim 10, nor would such a combination be proper relative to claim 1, as amended.

Claim Rejections – 35 U.S.C. § 103 – claims 4-13

The Examiner has rejected claims 4-13 under 35 U.S.C. § 103(a) as being unpatentable over Anma in various combinations with U.S. Patent Number 6,413,383 (Chiang *et al.*); U.S. Patent Number 6,972,209 (Agarwala *et al.*); U.S. Patent Number 3,887,993 (Okada *et al.*); and admitted prior art disclosed in the present application. Applicant respectfully traverses rejection of claims 4-13.

Each of claims 4-13, as amended, depends from independent claim 1. As discussed above, independent claim 1 is allowable. Claims 4-13 are also allowable at least by virtue of their dependence upon allowable claim 1. Accordingly, it is respectfully requested that the rejection of claims 4-13 under 35 U.S.C. § 103(a) be withdrawn.

CONCLUSION

In view of the foregoing amendment and remarks, Applicant respectfully submits that the present application, including claims 1-13, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted,

MICHAEL C. GAIDIS

December 18, 2006 By: _____
(Date)

KERRY GOODWIN
Registration No. 48,955
IBM CORPORATION
Dept. 18G
BLDG. 300-483
2070 Route 52
Hopewell Junction, NY 12533
Direct Dial: 845-892-9645
Facsimile: 845-892-6363
E-Mail: kerry.goodwin@us.ibm.com